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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,366	01/14/2004	Hiroaki Nakano	TAI 146	2358

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EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,366	NAKANO, HIROAKI	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 3005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 3, 6, 9, 12, 13, and 15 – 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Baba (US 6,046,077).

3. Regarding Claim 1, Baba discloses a circuit board for mounting a semiconductor chip, the circuit board including:

a semiconductor chip region (under chip 1, Figure 5B) of the circuit board (4) for mounting the semiconductor chip (1) and

wiring regions (not shown) (Col. 1, lines 58 – 60; Col. 3, lines 55 – 57) of the circuit board (4) in which wirings electrically connected to the semiconductor chip (through 12) are formed, the circuit board comprising:

a reinforcement layer region (6) of the circuit board (4) in which reinforcement layers for maintaining the strength of the circuit board for mounting the semiconductor chip (1) are formed, and

a protective film (3) (Figure 5D) that covers the wirings,

wherein the semiconductor chip region does not overlap the reinforcement layer region

(See Figure 5E).

4. Regarding Claim 2, as discussed in Claim 1, Baba discloses (Col. 1, lines 58 – 60; Col. 3, lines 55 – 57) that the semiconductor chip covers part of the wiring regions.

5. Regarding Claims 3, 12, and 13, Baba discloses that the reinforcement layers (6) are copper (conductive metal) wirings (Col. 1, lines 38 – 39).

6. Regarding Claim 6, Baba discloses a method of manufacturing a circuit board (4) including a semiconductor chip region (under chip 1) of the circuit board for mounting the semiconductor chip (1), a reinforcement layer region (under 6) of the circuit board in which reinforcement layers for maintaining the strength of the circuit board for mounting the semiconductor chip are formed, and wiring regions (not shown) (Col. 1, lines 58 – 60; Col. 3, lines 55 – 57) of the circuit board (4) in which wirings electrically connected to the semiconductor chip (through 12) are formed, the method comprising:

forming the wirings (12) in the wiring regions (not shown) (Col. 1, lines 58 – 60; Col. 3, lines 55 – 57) disposed in the vicinity of the semiconductor chip region (under 1),

forming a protective film (3) (Figure 5D) that covers the wirings,

wherein the semiconductor chip region (under 1) does not overlap the reinforcement layer (under 6) region (See Figure 5C).

Baba does not explicitly disclose that the reinforcement layers in the reinforcement layer region

are disposed in a vicinity of the wiring regions. However, Baba does disclose (Col. 1, lines 58 – 60) that the wiring layer is contained within the circuit board (4). Therefore it is inherent that the reinforcement layer (atop the circuit board) is disposed in a vicinity of the wiring regions.

7. Regarding Claim 9, Baba discloses a circuit board for mounting a semiconductor chip, the circuit board comprising:

an insulating substrate (4), the insulating substrate having a top surface and a bottom surface, with the top surface including mutually separated first, second and third regions of the substrate (See Marked-up Figure 5B).

wirings (12) provided in the second regions on the top surface of the insulating substrate with the semiconductor chip being electrically connected to the wirings,

reinforcement layers (6) provided only in the third region (See Marked-up Figure 5B) on the top surface of the insulating substrate, with the reinforcement layers maintaining the strength of the circuit board for mounting a semiconductor chip,

a protective film (3, 9,10) (Col. 3, line 63 through Col. 4, line 1) formed on the insulating substrate so as to cover the wirings and reinforcement layers, and

the semiconductor chip (1) mounted on the protective film (3) above the first region on the top surface of the insulating substrate (4),

wherein the third region encloses the first region and the second region (See Marked-up Figure 5B).

8. Regarding Claim 15, Baba discloses that solder balls (8) (Figure 5E) are disposed on the bottom surface of the insulating substrate (4) and electrically connected to the wirings.

9. Regarding Claim 16, Baba discloses that the wiring regions are disposed in the vicinity of the semiconductor chip region (under 1) and the reinforcement layer (under 6) region is disposed (Col. 1, lines 59 – 60) in the vicinity of the wiring regions.

10. Regarding Claim 17, Baba discloses (Col. 1, lines 58 – 60; Col. 3, lines 55 – 57) that wiring regions (7) are disposed between the semiconductor chip region (under 1) and the reinforcement layer region (under 6).

11. Regarding Claim 18, Baba discloses (Figure 5B) that the reinforcement layer region (under 6) encloses wiring regions (12) and semiconductor chip region.

Claim Rejections – 35 U.S.C. 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 4, 7, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baba, as applied to Claims 1 – 3, 6, 9, 12, 13, and 15 – 18, and further in view of Lin et al. (US 6,534,852 B1).

14. Regarding Claims 4, 7, and 10, Baba does not disclose the use of planarization on protect-ntive films. However, Lin et al disclose a circuit board/substrate for mounting a semiconductor chip, wherein the protective film (302g) is flat and planarized (See Figure 5E). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Baba and Lin et al. to obtain a flat even layer to reduce warpage and defect generation.

15. Claims 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baba, as applied to Claims 1 – 3, 6, 9, 12, 13, and 15 – 18, and further in view of Norville (US 6,534,852 B1).

16. Regarding Claims 5 and 8, Baba does not disclose the cutting and polishing of material to produce planarization. Norville discloses a fine polishing technique for slow removal of material from plastic (polymer) surfaces (Col. 4, lines 34 – 38), wherein a polishing apparatus is used with varying grades of abrasive compounds. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Baba and Norville to obtain a flat even layer to reduce warpage and defect generation.

17. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baba, as applied

to Claims 1 – 3, 6, 9, 12, 13, and 15 – 18,and further in view of admitted Prior Art of the instant application. Baba

does not disclose that the protective film is a solder resist. The use of solder masks for protective films is well known in the art. The Prior Art section of the Specification section of the instant application (p.2, lines 3 and 4 ; lines 20 – 23) disclose the use of solder resist as a protective film. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the admitted Prior Art of the instant application with Baba to obtain a protective mask for efficient packaging.

18. Claims 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baba, as applied to Claims 1 – 3, 6, 9, 12, 13, and 15 – 18, and further in view of Niwa (US 6,259,154 B1).

19. Regarding Claim 14, Baba does not disclose the use of insulating materials as reinforcement layers. Niwa discloses the use of insulating (resin) reinforcement layers (stiffeners) (21) (Figures 2C and 2E) (Col. 3, lines 57 – 60) for strength enhancement. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Baba with Niva to obtain a package with reduced weight (Niwa, Col. 5, lines 30 – 33).

20. Regarding Claim 19, Baba does not disclose that the wiring regions do not overlap the semiconductor chip region. Niwa discloses that wiring regions do not overlap the semiconductor chip region (2) (Figure 6)in a packaged structure. Since the lead structures and

interconnects are similar, it would have been obvious to one of ordinary skill in the art to use the lateral lead connection of Niwa in Baba to reduce complexity and processing steps.

Conclusions

21. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the

examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee
April 3, 2005